nffa.eu
PILOT 2021 2026

DELIVERABLE REPORT

WP13 - JA3 Nano-engineering and pattern transfer methods

D13.3

Atomic precision pattern transfer methods: performance and figure of merits

PROJECT DETAILS

PROJECT ACRONYM	PROJECT TITLE
NEP	Nanoscience Foundries and Fine Analysis - Europe|PILOT

GRANT AGREEMENT NO:	FUNDING SCHEME
101007417	RIA - Research and Innovation action

START DATE

01/03/2021

WORK PACKAGE DETAILS

WORK PACKAGE ID	WORK PACKAGE TITLE
WP13	JA3 Nano-engineering and pattern transfer methods

WORK PACKAGE LEADER

Assoc. Prof. Ivan Maximov (LUND)

DELIVERABLE DETAILS

DELIVERABLE ID	DELIVERABLE TITLE
D – 13.3	Atomic precision pattern transfer methods: performance and figure of merits

DELIVERABLE DESCRIPTION

The current deliverable D13.3 gives an overview of some important methods of pattern transfer in semiconductor nanofabrication where all 4 partners, LUND, EPFL, CSIC and C2N-CNRS are involved. The emphasis is put on atomic layer etching (ALE) that represent one of few approached in nano-processing that offer a potential of atomic layer control during removal of material. A related method of layer-by-layer epitaxial growth is added to give a more complete picture. Finaly, lithographic-based approaches of high-resolution patterning that do not yet provide atomic resolution are mentioned, too.

DUE DATE	ACTUAL SUBMISSION DATE
M32 (Month) 31/10/2023	31/10/2023

AUTHORS

Ivan Maximov (Lund), Andrea Cattoni (C2N-CNRS)

PERSON RESPONSIBLE FOR THE DELIVERABLE

Assoc. Prof. Ivan Maximov (Lund)

NATURE

- ☒ R - Report

- ☐ P - Prototype

- ☐ DEC - Websites, Patent filing, Press & media actions, Videos, etc

- ☐ O - Other

DISSEMINATION LEVEL

- ☒ P - Public

- ☐ PP - Restricted to other programme participants & EC: (Specify)

- ☐ RE - Restricted to a group   (Specify)

- ☐ CO - Confidential, only for members of the consortium

REPORT DETAILS

VERSION	DATE	AUTHOR(S)	DESCRIPTION / REASON FOR MODIFICATION	STATUS
1	18/10/2023			Draft
2	26/10/2023			Draft
				Choose an item.

CONTENTS

OUTLINE

The Joint Activity JA3 (WP13) has a focus on high-resolution lithographic methods combined with a pattern transfer, e.g. removal of material by reactive ion etching (RIE) and atomic layer etching (ALE). One of the main aims of current Joint Activity is the transfer of the developed technology of lithographic and patterning methods to the Transnational Access (TA) offer of the NEP project. The present Task concentrates on high-resolution patterning methods and include the milestone MS11, **ALE-based pattern transfer in Si structure with sub-10 nm resolution**.

Atomic layer etching provides layer-by-layer control in removal of semiconductor or dielectric materials and at the moment is the etching approach with the highest available accuracy. Without any doubt, the ALE represents (together with epitaxial growth methods, e.g. molecular beam epitaxy (MBE) and metalorganic vapor phase epitaxy (MOVPE)) one of few technological appproaches that can provide a real atomic layer control in nano-processing. Unlike lithographic techniques, where sub-task 13.2.2 belongs (see below), the ALE and epitaxy give atomic precision control in the vertical direction only. As for the lithography in general, atomic precision in the lateral direction is still out of reach, at least for practical applications. Of course, manipulation of atoms and molecules by e.g. scanning tunneling microscopes are well-known, but so far there was no real applications for those methods in the technology of nanostructures. Thus in the current report, we will focus on ALE as a representative method for etching with potentially atomic monolayer accuracy. The outcomes of the Task 13.2 will be used in the TA offer and possibly in other work packages such as WP14.

The Deliveable D13.3 embraces the **Task 13.2 "Pattern transfer with atomic precision"** and includes the following Subtasks:

Subtask 13.2.1: Atomic layer etching (ALE) (LUND, EPFL, CSIC)

ALE allows very fine control of the dry etching by a cyclic layer-by-layer material removal. We will develop a Cl-based ALE of Si combined with high-resolution lithography such as DSA and t-SPL to demonstrate a damage-free, sub-10 nm etching and explore a possibility to use ALE for dry resist development after He$^+$ FIB (Task 13.1). The ALE will also be used for expanding the capabilities of pattern transfer techniques offered in TA and in Task 13.3 and to test etching of III-Vs.

Subtask 13.2.2: High-resolution patterning by an additive approach (EPFL, LUND, CSIC)

t-SPL (Task 13.1) can be combined with lift-off for patterns < 20 nm without proximity effects and with high overlay accuracy. Approaches for this purpose include the use of bilayer and trilayer stacks, or by creating PPA bridges for shadow masks. The process will be optimized to include the new DLW option for multiple scale lift- off down to single-nm digit. This sub-task will also deal with selective modification of materials, using e.g. sequential infiltration synthesis of inorganic materials in BCPs (Task 13.1.2). Selective conversion of one polymer block in BCP to inorganic material will allow a high-resolution pattern transfer.

Another **Subtask 13.3.1: Selective-area growth of III-V nanowires** (C2N-CNRS, LUND, CSIC-CNM) is formally placed in **Task 13.3: Process integration, transfer to TA and applications.** However, in a broader sense, the selective area-growth of III-V nanowires can be regarded as a pattern transfer with atomic precision using so-called "bottom-up" nanofabrication

approach, where nanostructures (e.g. nanowires) are formed by self-organisation of atoms in epitaxial processes. Such epitaxial process can provide layer-by-layer (atomic) control over the grown material and will be briefly discussed in the current report.

Subtask 13.2.1: Atomic layer etching (ALE) (LUND, EPFL, CSIC)

The main difference of atomic layer etching (ALE) compared to other dry etching techniques, for example, reactive ion etching (RIE), plasma etching (PE) or ion beam etching (IBE) is the cyclic, self-limiting nature of the etching process[1–4]. It is the self-limiting steps that allow very accurate control of the etched material, to the atomic layer or monolayer (ML) precision[2].

A typical ALE scheme includes activation of the etched surface (e.g. Si) by introduction of a reactive gas (Cl_2), saturation of the surface to create covalent bonds between the gas molecules/atoms and the substrate atoms, removal of the excess gas molecules from the reaction chamber and finally, etching step by bombardment of the modified surface by energetic ions, for example, Ar^+ ions, Figure 1[5]. The ions provide sufficient energy to desorb the reaction products, like $SiCl_x$, but not to remove the uncontollable amount of underlayer substrate atoms (Si). As a result, at the end of the cycle, it is possible to remove a single monolayer of material that gives unprecedented accuracy and low damage effects in the etched substrate. The self-limiting step in this case is thermal adsorption of chlorine controlled by the Langmuir-Hinshelwood kinetics (molecular activation) or adsorption of Cl-radicals produced by Cl_2-plasma (atomic activation).
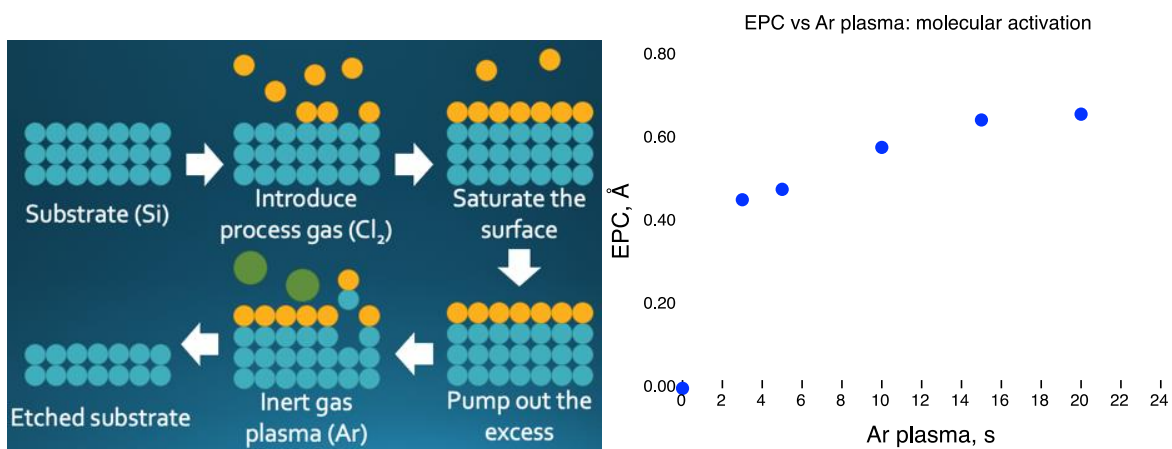

Figure 1: (Left) Schematic of the ALE of Si using Cl_2 as an etch gas. Adsorption of chlorine on the Si surface and its subsequent Ar^+ bombardment in plasma results in layer-by-layer etching mode. Removal of more than one monolayer during the bombardment is a characteristic of quasi-ALE process. (Right) The plot shows a typical self-limitation behavior of ALE etch per cycle (EPC) of Si as a function of Ar-plasma exposure time. The ALE process provided by molecular activation of Si surface by molecular Cl_2 adsorption.

Of course, it is clear that the ion energy must be fine-tuned in order to avoid unwanted sputtering of the substrate material by the physical ion bombardment. Substantial sputtering happens at a high energy range, typically above 30-50 eV - it depends on the etched material and the type of ions. In practice, however, it is difficult to completely avoid the sputtering effects and such atomic layer etching process with a significant contribution of ion beam sputtering or other "parasitic" effects is often called "quasi-ALE" process (Q-ALE). So the sputtering impact in a Q-ALE process will result in faster etch rate and a bit lower accuracy of etching. The etch per cycle (EPC) will gradually increase with the duration of ion bombardment in the etching step in Q-ALE, or will

saturate in "real" ALE, Figure 1. For ions with energy below the sputtering threshold, the ECP dependence on time of ion irradiation will show a saturation behavior[2].

Another contribution to the non-ideal ALE is presence of excess reactive gas in the gas phase of reaction chamber due, for example, to insufficient pumping time or excessively injected gas. The residual reactive gas molecules will dissociate and activate in Ar^+ plasma during the etching phase (see the step "Inert gas plasma (Ar) in Figure 1) to contribute with additional etch rate of the material. In the experiments, both sputtering and excess reactive gas give a significant contribution to the total etch rate and usually result in a decrease of reproducibility of the etching process.

For example, during our optimisation work of ALE process to etch Si with Cl_2 using Ar-plasma bombardment, the dosing of chlorine gas was reduced from the initial 20 sccm in the beginning of the experiments to 1-5 sccm and the Cl_2 pressure decreased from 60 to 3 mTorr in order to avoid the excess reactive gas in the chamber. As for the Ar^+ ion energy, that directly depends on the applied radio frequency (RF) power, the RF-power was reduced from 70 to 7-10 W. The reduction of both the injected amount of chroline and the ion energy allowed to adjust the EPC to the values that would be expected for a "real" ALE process, which is of the order of 0.5 Å, Figure 2.
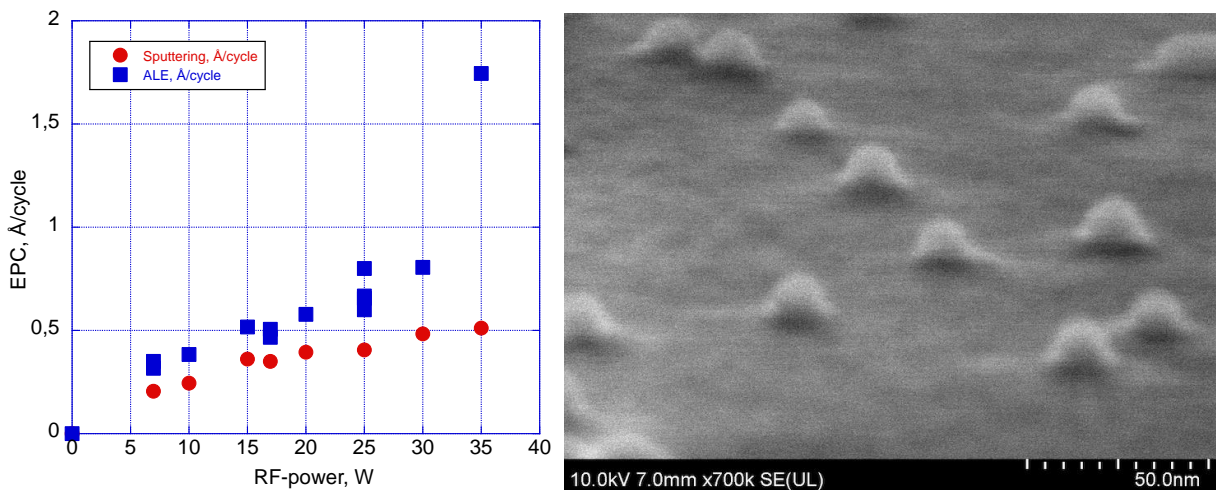

Figure 2: (Left) A plot of EPC as a function of RF-power that determines the Ar^+ ion energy (the plot is adopted from the report on MS11). The red circles show the physical sputtering contribution, while the blue squares indicate the total etching rate. (Right) An example of ALE of Si using nominally 25 nm Au aerosol particles with the final etched features of about 10 nm in diameter, that indicate a strong mask erosion.

The performance of ALE is determined by many etch process parameters, but the most important are (a) the ion energy (controlled by the RF-power and pressure), (b) the amount of injected reactive gas (controlled by gas flow, pressure and the injection duration), (c) time of ion bombardment and other factors. It was found that the "process window" where the ALE can be successfully used is usually very small, for example, high ion energy may result in degradation of etch masks. Figure 2 shows a scanning electron microscope (SEM) image of the etched Si pillars where 25 nm aerosol Au particles were used as etch masks. The measured size of the etched Si structures is about 10 nm that indicate that the aerosol Au particles were eroded during the ALE process. Smaller particles or longer etch cycles resulted in complete disappearance of the masks. The erosion was most likely caused by the Ar^+ ion sputtering, since gold does not form volatile compounds under the condition used in ALE.

Below is a basic analysis of atomic layer etching performance and the figures of merits of the technique and its comparison with other common etch methods, like RIE. In particular, the following parameters will be presented and compared:

- absolute etching rate
- accuracy of etching
- etch selectivity
- damage effects during etching

Please bear in mind that this analysis is based on our experimental JA activity and some literature reviews and will be updated in due course.

Subtask 13.2.2: High-resolution patterning by an additive approach (EPFL, LUND, CSIC)

In contrast to the atomic layer etching where the material removal process can be controlled with an accuracy of a single monolayer in the vertical direction, horizontal (lateral) patterning with the same precision is extremely difficult to implement. The closest solution would be a manipulation of atoms or molecules using scanning tunneling microscope, but this approach has no practical significance for practical nano-technology and will not be considered here.

Thermal scanning probe lithography (t-SPL) is one of the lithographic techniques that allows sub-10 nm features[6]. The t-SPL is based on local heating of an atomic force microscope (AFM) tip that results in sublimation of a suitable resist film. The EPFL group together with CSIC-CNM demonsrated a lift-off process with sub-20 nm features combined with direct laser write (DLW) for patterning 2D materials and t-SPL nanopatterning on silicon nanowires (Milestone MS26). Figure 3 illustrates an example of a fabrication process to make MoS_2-based filed-effect transistor (FET) using the t-SPL and DLW.
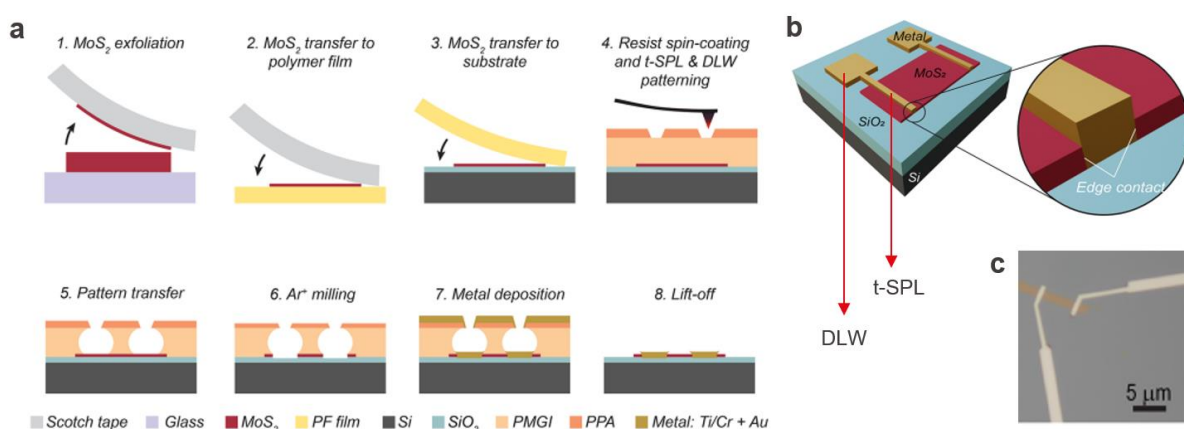

Figure 3: (a) The process flow to fabricate 2D-FET in 2D material. (b) Combined t-SPL and DLW for forming source-drain and contact pads. Details of the process are in the MS26 report.

Another additive patterning approach includes block-copolymer (BCP) lithography combined with sequential infiltration synthesis (SIS) to produced e.g. ultra-high resolution etching masks for reactive ion etching or atomic layer etching. The BCP lithography allows formation of regular patterns with single-nanometer resolution, especially when BCP-materials with high Flory-Huggins interaction parameter are used. In the present work we demonstrated sub-10 nm patterning of Si

substrate using Polystyrene-b-Maltoheptause (PS-b-MH)[7,8] and Polystyrene-b-Poly(4-vinyl pyridine) (PS-b-P4VP). An optimised sequential infiltration synthesis is used on those BCP films to form etch masks to be used in a F-based reactive ion etching.
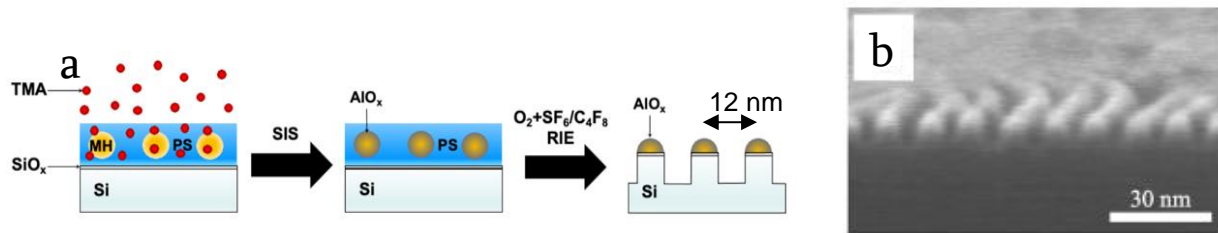

Figure 4: (a) Schematic illustration of sequential infiltration synthesis of AlO_x in the MH block in PS-b-MH BCP film and (b) Scanning electron microscoscopy (SEM) cross-section of a Si sample after its reactive ion etching using alumina as an etch mask. Etched features of about 6 nm were achieved[8].

Figure 4 shows a schematic of the SIS process in PS-b-MH BCP film and the final result of a high-resolution reactive ion etching of Si when the AlO_x served as an etch mask. The BCP-RIE technology described here can be regarded as a combined additive and subtractive process.

Subtask 13.3.1: Selective-area growth of III-V nanowires (C2N-CNRS, LUND, CSIC-CNM)

The possibility to grow high structural quality III-V nanowires (NWs) on mismatched substrates, represents an elegant way to integrate III-V materials on Silicon for example to fabricate a III-V on Si tandem solar cell avoiding in one go the use of expensive III-V substrates and the difficult integration of III-V on Si. The selective area growth of III-V NW is typically obtained by pattering a thin SiO_2 (or SiN) mask on Si(111) substrate by electron beam, nanoimprint or Talbot lithography and dry etching and the selective growth us performed by Vapor-Liquid-Solid (VLS) method using a Gallium catalyst (self-catalyzed growth) by MBE or MOVPE. The two main problems using this method are the difficulty in obtaining reproducibly high yield of vertical NWs[9,10], and the difficulty to tune the NWs diameters, which tend – independently from the nanohole opening diameter and the Ga-droplet dimensions – to converge to 80-90 nm diameter.

In the framework of the NEP project, we have optimized the fabrication of the SiO_2 mask to solve these two issues obtaining high (100%) yield of vertical NWs and the tuning of the NWs diameters from the beginning of the growth (that is, using only VLS growth without any contribution of Vapour Solid growth as reported in the past). The Si(111) surface is first cleaned by three successive cycles of oxidation in oxygen plasma reactive ion etching (RIE) and etching in hydrofluoric acid (HF) diluted in water to 5% concentration. This first cleaning procedure of the Si surface is key to obtain high yields of vertical NWs yet not sufficient to achieve homogeneous high yields over the whole surface of a 2 inches wafer, Figure 5.
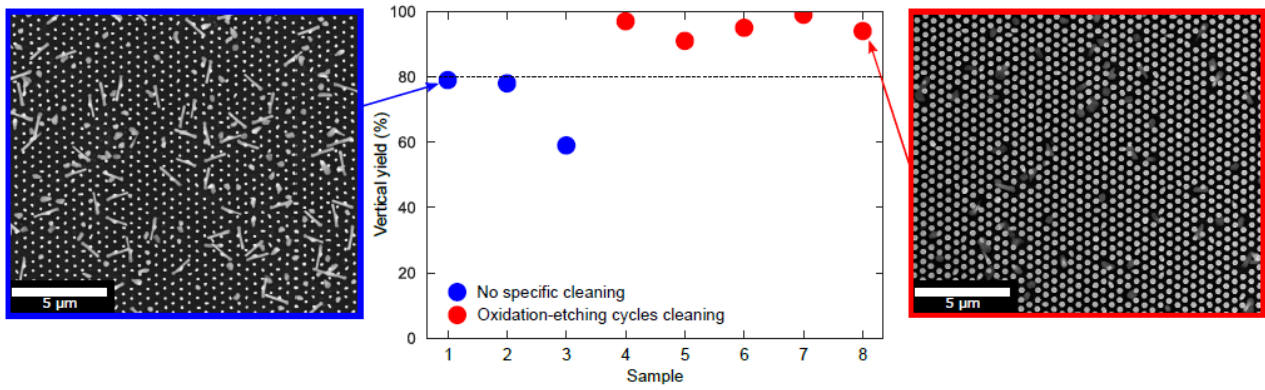
Figure 5: Influence of the Si wafer oxidation-wet etching cycles on the NW vertical yield. Various GaAs NW samples were grown with a similar GaP foot on Si(111) wafers coated with a thin layer of SiO_2 (subsequently patterned). Before the SiO_2 layer deposition, the Si wafers are cleaned with either a simple HF dip (blue), or a cleaning procedure consisting of 3 cycles of plasma oxidation and HF etching (red). The vertical yield was estimated in the middle of the 1.5×1.5 cm^2 NW array, centered on 2" Si wafers. SEM top-view images of two representative samples are shown. The different NW morphologies come from different shell thicknesses. Figure reprinted from[11].

A 70 nm thick silica layer is deposited via plasma-enhanced chemical vapor deposition (PECVD). We have worked on the SiO_2 deposition process in order to achieve low carbon contamination (not shown). The mask was the then patterned by e-beam lithography (hexagonal array of hole apertures with 8 different diameters), pattern transfer by RIE (SF_6/CHF_3) and the remaining SiO_2 layer inside the nanoholes holes removed by a dip in a 1% water HF solution. GaAs NWs growth was carried out in a Riber Compact 21 MBE system at 600 °C using a predisposition step of Ga, a short GaP stem (40 nm) followed by the GaAs growth by the VLS method. Ga pre-deposition time and III/V ratio must be tuned according to the final NW diameter and the required taper.

For relatively short growth times (8 minutes in this case), NW with different diameter can be grown during the same epitaxial growth having all a vertical yield approaching 100%. This is the first time that the diameter of self-catalyzed III-V NWs on Si are controlled by VLS, from the beginning of the growth, Figure 6.

While high yields of vertical NWs approaching or reaching 100% can be achieved "locally" using these process parameters, we observed inhomogeneous yields over the 2. We attributed this inhomogeneity to the contaminants introduced on the substrate surface during DI water rinsing after the final HF1% step and left there by the standard N_2 blow-drying. In fact, a considerable amount of water evaporation occurs during blow-drying, and contaminants initially dissolved in the evaporated water can be left behind and cause undesirable drying marks[12].
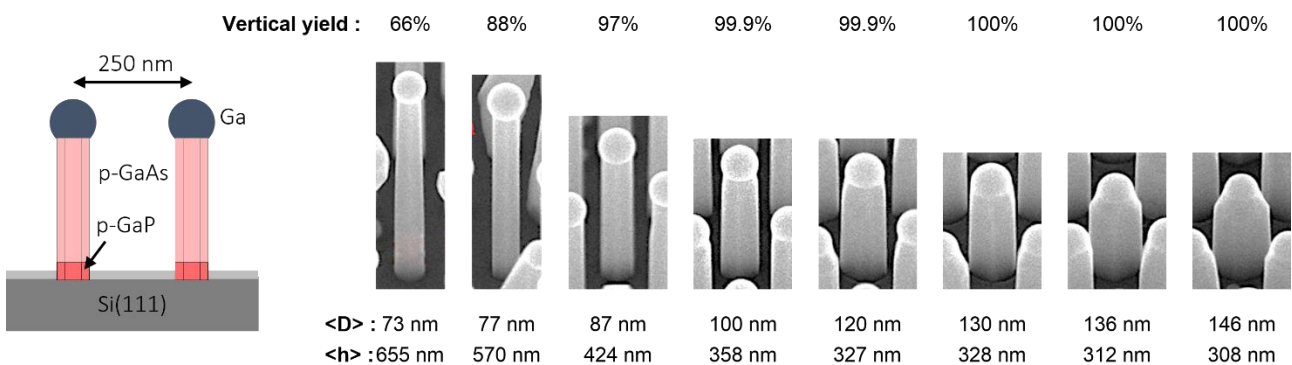
Figure 6: SEM images of representative NWs grown with different average diameters <D>, average height <h> and the corresponding yield of vertical NWs. The average diameters and heights were measured on 10 different NWs per group.

To solve the problem, we implemented a Marangoni drying process for SiO_2 (Marangoni drying is typically used microelectronics industry to properly dry Si wafers). The fundamental difference between a Si and a SiO_2 surface is that while the former is hydrophobic, the latter is hydrophilic. For this reason, we implemented a Marangoni drying using a dip-coater in which the patterned SiO_2 samples (after the HF1% step) are dried in a N_2/2-methoxyethanol atmosphere while the enclosure containing the wafer withdrawn from a DI bath is kept at 105 °C to ensure a complete evaporation of the DI from the SiO_2 surface (in the very same way it occurs for hydrophobic Si at room temperature). The sample is the transferred in the MBE for NWs growth without any additional drying step.

Figure 7 (b) shows the results: an average yield of vertical NWs of 99.5% is obtained over a 2" surface area (as the patterning of the whole 2" wafer is time consuming, we patterned 7 areas of $1mm^2$ in the different position of the 2" wafer).
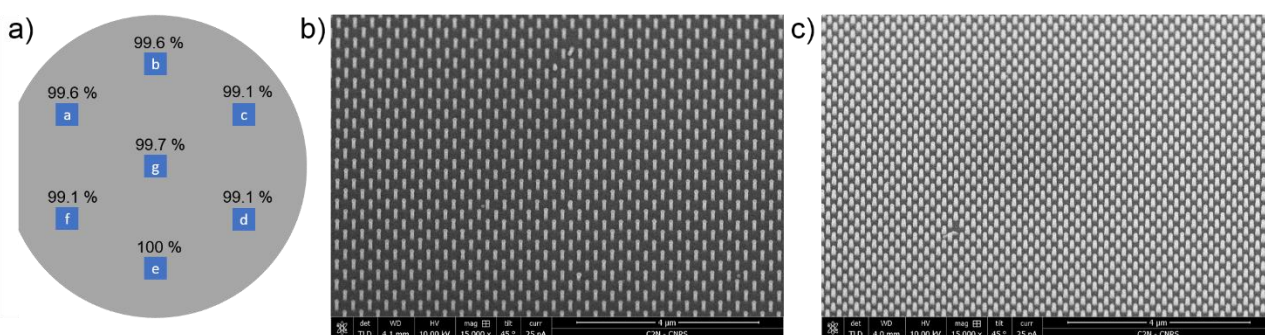

Figure 7: Results obtained on the sample processed using the modified Marangoni drying **a)** Schematic of the 7 patterned areas of 1 mm^2 on a 2 inches Si substate with the corresponding yields of vertical NWs measured. **b/c)** Representative SEM images from the pattern "a" with two different periods (360/250 nm).

PERFORMANCE AND THE FIGURE OF MERIT

Subtask 13.2.1: Atomic layer etching (ALE)

Absolute etching rate: the absolute etching rate of ALE is very low due to the fact that only a single monolayer (ML) or several monolayers (Q-ALE) are etched away in the etch cycle. In the one of the most studied process, atomic layer etching of Si, the values of EPC may differ by an order of magnitude, from 1 to tens of Å[4,13,14]. In our experiments the EPC of Si with Cl_2 as the reactive gas and Ar^+ plasma, vary from approximately 0.3 to 1.7 Å, Figures 1 and 2. Our earlier experiments demonstrated even higher etch rate, up to 8.5 Å/cycle, but it is clear now that the fast etching was due to high Ar^+ ion energy, exceeding 60 eV and the excess of Cl_2 gas. Other authors reported a wide variation of Si etching rate using, apart from Cl_2, a different chemistry,

for example, CF_4/O_2, NF_3/He[1]. However, it is not uncommon to report EPC of several Å, that clearly indicate a quasi-ALE regime[5,13].

Taking into account the duration of each ALE step, that have been optimised, namely: (a) surface activation 5 s, (b) purge 40 s, (c) Ar plasma bombardment 10 s and (d) etch purge 2 s, the whole ALE cycle takes 57 s. Assuming a reasonable EPC of 1 Å, one can estimate the ALE absolute etching rate of Si to be about 6 nm/hour. This can be compared to a typical etching rate used in reactive ion etching processes for nanofabrication of 100 nm/min that equals to 6 μm/hour[15]. This is a very rough comparison, but it shows that the real ALE is about 1000 times slower in comparison with the conventional RIE processes. Thus this simple calculation explains the interest of the world-wide ALE community towards the Q-ALE processes that offer about ten time faster etching rate compared to the real ALE. However, as a result, the higher etching rate the Q-ALE processes may not offer the atomic layer etch control.

In discussion about the etching rates of different methods, one should not forget that the ALE is the only etching technique that potentially allows atomic resolution, so its application area includes formation of structures and devices with sub-10 nm feature size. As a consequence, the absolute etching rate of ALE may not play so big role in comparison with traditional etching techniques, like RIE.

Accuracy of the etching process: the low etching rate of ALE and its cyclic process make it possible to stop the etching when the exact number of MLs is removed, while the traditional RIE will have to rely on duration of the process or *in-situ* measurements, e.g. optical emission or mass-spectroscopy. While the ALE makes use of self-limiting steps, for example, adsorption of reactive gases, that result in low sensitivity to process variations, the RIE may suffer from instabilities of startup of plasma discharges, that may affect the etching rate. So in practice the ALE etch accuracy in vertical direction is superior to RIE may be of order of 1 Å.

Surface ML adsorption of reactive gas species during molecular or atomic activation in ALE provides a perfect condition for uniform etching rate over the whole area of the specimen. On the contrary, the etch uniformity in RIE depends upon plasma density at a given place of the sample and may vary depending on hardware design or process conditions.

The accuracy of etching can also be described in terms of surface roughness (rms), and in many cases this is a critical parameter, especially for structure sizes well below 100 nm. There are a number of reports about supervior surface quality obtained after ALE[2]. Our recent data where a RIE with Cl_2/Ar and ALE with the same chemistry were used to etch Si, indicated that the rms of Si surface after RIE was between 0.2-0.4 nm, while ALE produced a very smooth surface with rms of 0.1 nm[16].

Etch selectivity: the etch selectivity can be defined as a ratio of etching rate of substrate to the etching rate of a protective mask. In an ideal case the mask is not etched at all, giving the infinite etch selectivity. In practice, however, typical etch selectivity is between 2:1 and 10:1, and it depends on the mask material and the etching conditions. For example, silicon dioxide is a perfect protective mask in Si etching in a Cl-based chemistry with selectivity better than 10:1.

In our experiments, with the following mask types: (a) photoresists PAR/PMGI, (b) block-copolymers with selectively infiltrated alumina, (c) aerosol particles of Au and Pd, the ALE process was used to etch Si. The photoresists were utilised during the initial experiments with a high RF-power and excess Cl_2 flows, so the etching conditions were Q-ALE with strong effects of high Ar^+ energy and gas-phase chlorine RIE. Unfortunately, there is no data from a corresponding RIE to compare with the ALE, but the SEM cross-section inspection indicated a significant erosion of the

photoresist masks after 200 cycles of ALE. The top PAR resist was almost completely removed during the process, so the etch selectivity can be estimated as 1:1. Such selectivity can be observed in a conventional Cl_2/Ar inductively-coupled RIE of Si. In joint experiments between LUND and CSIC-CNM to apply the ALE process to etch or modify the Si nanowires, it was found that a negative resist used to form the etch mask was eroded during the chlorine/argon ALE process. The modified resist cross-linked in etching to make it difficult to remove by conventional solvents. At the same time, we discovered that the atomic layer etching results in a much smoother surface compared to RIE.

An attempt has been made to test infiltrated block-copolymer (BCP) of polystyrene-b-poly(4-vinyl pyridine) – PS-b-P4VP, where P4VP block is infiltrated by sequential infiltration synthesis (SIS) using trimethylaluminum and water to convert the P4VP polymer block to Al_2O_3[8,17]. The alumina mask is well-known for its high stability in an agressive environment, e.g. halogen gases. After the SIS, the samples was etched by a low-power ALE process with reduced amount of chlorine. The etch selectivity of 15-20 nm large alumina masks on Si wafer was not sufficient for a relaibe pattern transfer, that could be due to a porous structure of the mask[17].

Aerosol-generated 25 nm particles of Au and Pd were also tried for the masking applications. In this case, the etch selectivity of the 25 nm Au particles was found to be enough to etch ≈10 nm Si pillars. At the same time, the size of the particles decreased from 25 to 10 nm after only 50 cycles of etching in ALE. Figure 8 shows a significant decrease in size of the aerosol Au particles, from roughly 25 to 10 nm, after the ALE.

In conclusion, our ALE process showed a limited etch selectivity, at least with the three tested types of masks. The best results were obtained with the aerosol Au particles, but even those particles were eroded to about half of their original size. One of possible reasons for the poor etch selectivity with those materials can be a significant influence of the ion bombardment that non-selectivily removed both Si and the mask material.
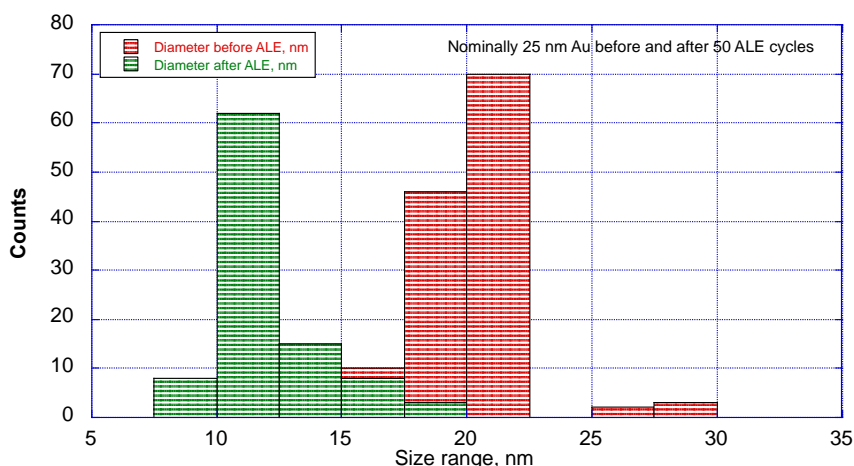

Figure 8: Size distribution of 25 nm Au aerosol masks before and after 50 cycle of ALE of Si using Cl_2 and Ar chemistry.

Damage effects in ALE: So far the damage effects in ALE were not covered very well in literature, so the knowledge here is limited. However, one can expect a lower degree of substrate damage in an atomic layer etching process compared to a traditional RIE process because of (a) a cyclic nature of ALE and (b) very low energy of the impinging ions. Some recent publications on molecular dynamics (MD) modelling of ALE, indicate that during bombardment of Si surface with 20 eV Ar^+ ions, the damaged layer stretches to about 1.2 nm, Figure 9 (left)[18]. At the same time,

there are no extensive experimental studies of ALE-related damage effects in semiconductors, few papers point out low degree of damage in III-V semiconductor structures during ALE[19,20].

Our recent studies of ALE of Si using chlorine and argon demonstrated a relatively low energy of Ar⁺ ions during the etching step, Figure 9 (right). As can be seen in the figure, the Ar⁺ ions have a peak energy of 39-55 eV, that is sufficient for the ALE process and significantly less than the corresponding energy in a typical RIE process (100-300 eV).
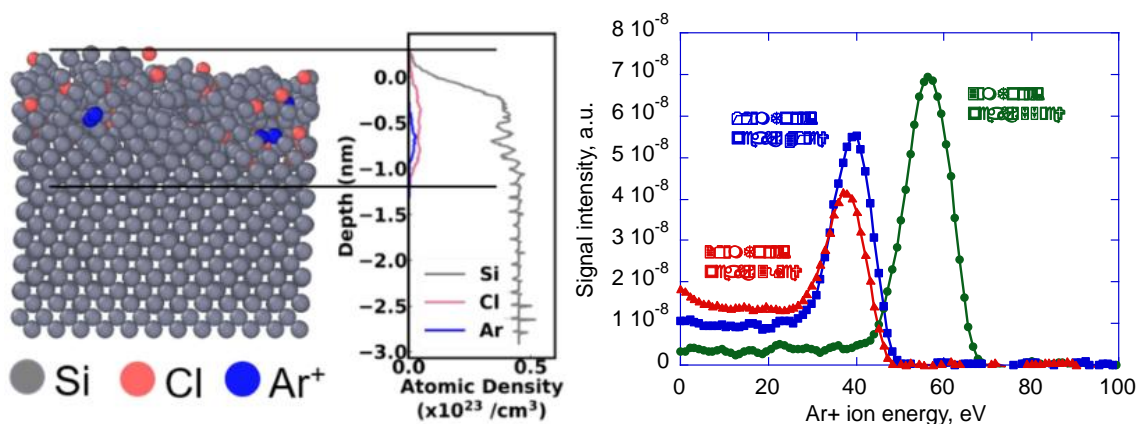

Figure 9: (left) Molecular dynamics simulation of atomic configuration and corresponding atomic density profiles for Si, Ar and Cl atoms after one cycle of ALE with atomic Cl* activation and Ar+ ion energy of 20 eV[18]. (Right) Dependence of Ar⁺ ion energy on Ar gas pressure during the RF-plasma discharge with the DC-bias set to 7 V in PlasmaTherm Takachi™ RIE tool. Increase of Ar gas pressure from 3 to 20 mTorr results in reduction of Ar⁺ energy distribution peak from 55 to 39 eV. The ion energy must be adjsted to reach the ALE regime, but the ions may also be responsible for generation of surface damage.

The latest preliminary data of LUND obtained by Kelvin Probe Force Microscopy (KPFM) indicate less damage in Si during ALE compared to RIE[16]. The Si surface potential as measured by KPFM, demonstrated values of the surface potential close to the unetched reference Si (4.7 V) after ALE, while the conventional RIE process with the same chemistry resulted in a significant reduction of the potential to 4.1 V.

Subtask 13.2.2: High-resolution patterning by an additive approach

The two above-mentioned additive lithographic patterning, t-SPL and BCP-lithography, in combination with lift-off or SIS, do not yet provide atomic precision of the lateral patterning. As with other high-resolution lithographic methods, e.g. electron beam or ion beam lithography, those techniques are capable to single-digit (<10 nm) nanopatterning, however, they have their own limitations. Both have unique advantages and disadvantages which are briefly discussed below.

Thermal scanning probe lithography (t-SPL): the lateral resolution of t-SPL is generally limited by the tip diameter and heat spreading, but it is possible to achieve single-digit pattern transfer using t-SPL when thin resist layer is used[21]. Due to the small aspect ratio of features in the PPA polymer, thickness of the resist film must be very small, 5-10 nm. As a result, typical approach to transfer patterns from the PPA resist after the t-SPL, includes patterning of a thin dielectric film of SiO_2 that can serve a reliable etch mask in the following etching step. The aspect

ratio in t-SPL can be improved by the ultra-sharp tip with high aspect ratio, that can be produced by e.g. electron or ion beam enhanced deposition of metal on the standard t-SPL tip (Subtask 13.3.3). Throughput of the t-SPL is relatively low and comparable with that of atomic force microscope, however, the possibility to image the area to be patterned for e.g. mix and match lithography is a big advantage of t-SPL.

Block-copolymer (BCP) lithography: this lithographic method can be combined with SIS modification to allows formation of sub-10 nm regular features on large area using a self-organisation of a BCP films on the substrate surface[22]. Very often the block copolymers aree used in combination with directed self-assembly (DSA) that improves the patterning[23]. Resolution of the BCP-lithography depends on the Flory-Huggins parameter, the big parameter allows formation of small structures, less than 10 nm. At the same time, this technique can only be used for formation of regular patterns, e.g. hexagonally-arranged holes or arrays of lamellas[22]. High-resolution additive patterning in block-copolymers can be realised by a number of techniques, including lift-off or sequential infiltration synthesis[8,24], but the final resolution will depend on the BCP pattern. Throughput of BCP-approach is fairly high, since it is a parallel patterning method, however, one of the major problems is defectivity of the copolymer film. As in t-SPL, the BCP approach relies on very thin films for a high resolution, a single-digit patterning requires typically sub-20 nm film thickness, that limits how the patttttern can be transfered into the substrate. The SIS approach is a promising technique, however, it has its own limitations due to a high porosity and low density of AlO_x films, that reduces stability of the dielectric in e.g. dry etching[17].

Subtask 13.3.1: Selective-area growth of III-V nanowires

Epitaxial growth of III-V nanowires (NW) is related to ALE due to its ability to control the vertical growth of the material with atomic precision. However, the lateral patterning to control the size and position of NW is usually performed by conventional high-resolution lithography, e.g. electron beam lithography as demonstrated in Subtask 13.3.1. There were attempts to apply BCP-defined masks for selective growth of InAs NW, in this case the lateral size of NWs is determined by the BCP-lithography, DSA guiding lines and their orientation[23]. Here it was possible to control the orientation of the vertical InAs NWs relative to eahc other, that may be of interest for NW device applications.

REFERENCES

[1] G.S. Oehrlein, D. Metzler, and C. Li, "Atomic Layer Etching at the Tipping Point: An Overview," Ecs J Solid State Sc **4**(6), N5041–N5053 (2015).

[2] K.J. Kanarik, S. Tan, and R.A. Gottscho, "Atomic Layer Etching: Rethinking the Art of Etch," The Journal of Physical Chemistry Letters **9**(16), 4814–4821 (2018).

[3] F. Rahman, and J.C. Runyon, "Atomic Layer Processes for Material Growth and Etching A Review," Ieee T Semiconduct M **PP**(99), 1–1 (2021).

[4] S.A. Khan, D.B. Suyatin, J. Sundqvist, M. Graczyk, M. Junige, C. Kauppinen, A. Kvennefors, M. Huffman, and I. Maximov, "High-Definition Nanoimprint Stamp Fabrication by Atomic Layer Etching," ACS Applied Nano Materials **1**(6), 2476–2482 (2018).

[5] Y. Ilarionova, Real- and Quasi-Atomic Layer Etching for Ultra-High Resolution Patterning, MSc-thesis, Lund University, 2022.

[6] S.T. Howell, A. Grushina, F. Holzner, and J. Brugger, "Thermal scanning probe lithography—a review," Microsyst. Nanoeng. **6**(1), 21 (2020).

[7] I. Otsuka, N. Nilsson, D.B. Suyatin, I. Maximov, and R. Borsali, "Carbohydrate-based block copolymer systems: directed self-assembly for nanolithography applications," Soft Matter **13**(40), 1–6 (2017).

[8] A. Löfstrand, R.J. Jam, K. Mothander, T. Nylander, M. Mumtaz, A. Vorobiev, W.-C. Chen, R. Borsali, and I. Maximov, "Poly(styrene)- block -Maltoheptaose Films for Sub-10 nm Pattern Transfer: Implications for Transistor Fabrication," Acs Appl Nano Mater **4**(5), 5141–5151 (2021).

[9] S. Plissard, G. Larrieu, X. Wallart, and P. Caroff, "High yield of self-catalyzed GaAs nanowire arrays grown on silicon via gallium droplet positioning," Nanotechnology **22**(27), 275602 (2011).

[10] E. Uccelli, J. Arbiol, C. Magen, P. Krogstrup, E. Russo-Averchi, M. Heiss, G. Mugny, F. Morier-Genoud, J. Nygård, J.R. Morante, and A.F. i Morral, "Three-Dimensional Multiple-Order Twinning of Self-Catalyzed GaAs Nanowires on Si Substrates," Nano Lett. **11**(9), 3827–3832 (2011).

[11] R. de Lepinau, GaAs-on-Si Solar Cells Based on Nanowire Arrays Grown by Molecular Beam Epitaxy, 2020.

[12] K.L. Mittal, *Particles in Gases and Liquids 3: Detection, Characterization, and Control* (Springer US, 2013).

[13] S. Tan, W. Yang, K.J. Kanarik, T. Lill, V. Vahedi, J. Marks, and R.A. Gottscho, "Highly Selective Directional Atomic Layer Etching of Silicon," Ecs J Solid State Sc **4**(6), N5010–N5012 (2015).

[14] S.-D. Park, K.-S. Min, B.-Y. Yoon, D.-H. Lee, and G.-Y. Yeom, "Precise Depth Control of Silicon Etching Using Chlorine Atomic Layer Etching," Jpn J Appl Phys **44**(1R), 389 (2005).

[15] K. Nojiri, *Dry Etching Technology for Semiconductors* (Springer, 2015).

[16] M. Alabrash, Damage Analysis of Reactive Ion and Atomic Layer Etched Silicon, MSc-thesis, Lund University, 2023.

[17] A. Löfstrand, A. Vorobiev, M. Mumtaz, R. Borsali, and I. Maximov, "Sequential Infiltration Synthesis into Maltoheptaose and Poly(styrene): Implications for Sub-10 nm Pattern Transfer," Polymers-Basel **14**(4), 654 (2022).

[18] E.J.C. Tinacba, M. Isobe, and S. Hamaguchi, "Surface damage formation during atomic layer etching of silicon with chlorine adsorption," J Vac Sci Technology Vac Surfaces Films **39**(4), 042603 (2021).

[19] H. Fukumizu, M. Sekine, M. Hori, K. Kanomaru, and T. Kikuchi, "Atomic layer etching of AlGaN using Cl2 and Ar gas chemistry and UV damage evaluation," Journal of Vacuum Science & Technology A **37**, 021002 (2019).

[20] S. Nakamura, A. Tanide, T. Kimura, S. Nadahara, K. Ishikawa, O. Oda, and M. Hori, "GaN damage-free cyclic etching by sequential exposure to Cl2 plasma and Ar plasma with low Ar+-ion energy at substrate temperature of 400 °C," J Appl Phys **133**(4), 043302 (2023).

[21] Y.K.R. Cho, C.D. Rawlings, H. Wolf, M. Spieser, S. Bisig, S. Reidt, M. Sousa, S.R. Khanal, T.D.B. Jacobs, and A.W. Knoll, "Sub-10 Nanometer Feature Size in Silicon Using Thermal Scanning Probe Lithography," ACS Nano, acsnano.7b06307-9 (2017).

[22] C. Cummins, T. Ghoshal, J.D. Holmes, and M.A. Morris, "Strategies for Inorganic Incorporation using Neat Block Copolymer Thin Films for Etch Mask Function and Nanotechnological Application," Advanced Materials **28**(27), 5586–5618 (2016).

[23] A. Löfstrand, R.J. Jam, J. Svensson, A. Jönsson, H. Menon, D. Jacobsson, L. Wernersson, and I. Maximov, "Directed Self-Assembly for Dense Vertical III–V Nanowires on Si and Implications for Gate All-Around Deposition," Adv Electron Mater, (2022).

[24] A. Löfstrand, R.J. Jam, M. Mumtaz, K. Mothander, T. Nylander, A. Vorobiev, A. Rahaman, W.-C. Chen, R. Borsali, and I. Maximov, "Sequential infiltration synthesis and pattern transfer using 6 nm half-pitch carbohydrate-based fingerprint block copolymer," Adv Patterning Mater Process Xxxviii **11612**, 116120W-116120W–9 (2021).